

## **IN THE CLAIMS**

***Kindly replace the claims of record with the following full set of claims:***

1. (Currently amended) Integrated circuit having a plurality of processing modules (M, S) and an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a packet based communication based on transactions between said plurality of processing modules (M, S), wherein each packet comprises a first predetermined number of subsequent words each having a second predetermined number of bits, wherein a first of said plurality of processing modules (M) issues a transaction by sending at least one packet over said interconnect means to a second of said plurality of processing modules (S), comprising:

at least one packet inspecting unit (PIU) for inspecting bits of said at least one packet to determine bits not required for said issued transaction and for matching said not required bits in a header of said at least one inspected packet related to a path over said interconnect with corresponding bits of a following ~~another~~ word within the same packet.

2. (Cancelled).

3. (Cancelled)

4. (Currently amended) Integrated circuit according to claim ~~[[2]]~~ 1, further comprising:

- at least one network interface (NI) associated to said first of said plurality of

processing modules (I) for controlling the communication between said first of said plurality of processing modules (I) and said interconnect means (N), wherein each of said at least one packet inspecting units (PIU) is arranged in one of said network interfaces (NI).

5. (Currently amended) Method for packet switching control in an integrated circuit having a plurality of processing modules (M, S) and an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a packet based communication based on transactions between said plurality of processing modules (M, S), wherein each packet comprises a first predetermined number of subsequent words each having a second predetermined number of bits, wherein a first of said plurality of processing modules (M) issues a transaction by sending at least one packet over said interconnect means to a second of said plurality of processing modules (S), comprising the steps of:

- inspecting bits of said at least one packet to determine bits not required for the issued transaction and updating said not required bits of said at least one inspected packet with corresponding bits of a following ~~another~~ word of the same packet, wherein said unused bits are related to a path over said interconnection.